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DESIGN OF ULTRA LOW-POWER 16-BIT CARRY SELECT ADDER USING FULLY SYMMETRICAL BRIDGE STYLE CIRCUIT

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Abstract- The addition is a basic arithmetic operation and act as the core of other arithmetic operations like multiplication, division, subtraction, address generation etc. Adders are the key element in many VLSI systems such as microprocessors,Arithmetic and Logic Units (ALU's), multiplexers, digital signal processing (DSP) architectures etc.As the technology node goes down, requires an efficient and robust full adder that can perform well even with the low supply voltages .In this paper designed a new 16 bit Carry Select Adder (CSLA) using fully symmetrical bridge style full adder circuit that can perform much well than the regular CMOS design in terms of power consumption at low voltages.The proposed CSLA was compared with conventional CMOS full adder CSLA in terms of power and delay.The design and simulation is done in Cadence gpdk 90nm Technology.
Keywords- CSLA, Fully Symmetrical Bridge Style,Transmission Gate (TG) Multiplexer.

1. INTRODUCTION

As the demand of low power circuits increasing in the modern days,design of power efficient logic systems has became the most important areas of research in VLSI system design.The digital can perform many types of logical functions,the main among them is the addition operation.As addition is most extensively used operation in many general purpose processors to application specific DSP Processors.As this addition operation can be done by using various types of adders such as Ripple Carry Adder,Carry Look Ahead Adder,Carry Select Adder etc.

The speed of the digital adder mostly determined by the amount of time required to propagate the carry through adder also called as propagation delay.This delay is different in different types of adders.CSLA is one of the fastest adders in which MSB is designed assuming once carry as '0' and carry as '1' i.e., multiple carries are independently generated and selects a suitable carry to generate sum.

This paper organized as follows. Section 2 describes the types of existing adder structures.Section 3 demonstrates the conventional 16-bit CSLA design using conventional 2x1 multiplexer.Section 4 demonstrates the design of proposed 16-bit CSLA using TG multiplexer.Section 5 contains simulation results and discussions. Section 6discuss the conclusion and future works followed by comparison table.

2. TYPES OF ADDERS

2.1 Ripple Carry Adder:

Ripple Carry Adder is designed by cascading the full adders in series that is the carry of first full adder is given to second and the carry of second full adder is given to third and so on.The Sum's are calculated at each full adder whereas the carry is taken at the the final full adder.As this adder is easy to design ,it suffers from great dealy as the next cascaded full adder has to wait for the carry from its previous adder which increases delay.Despite of its easy design ,this adder is not widely preferred due to its large delay drawback.A four bit ripple carry adder fig.1 .Ripple carry adder waits for the input carry (Ci) and then computes Sum and Carry out (Co).

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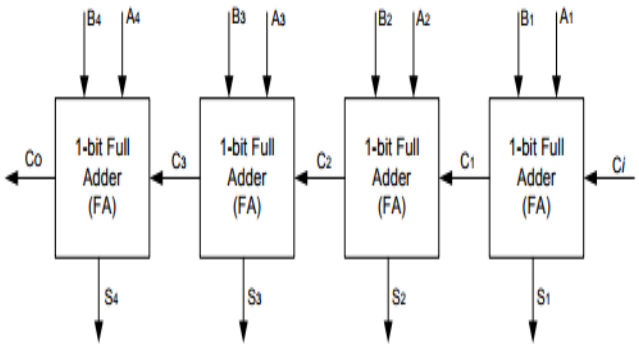


Fig.1:Ripple Carry Adder

2.1 Carry Select Adder:

In order to reduce the delay Carry Select Adder is introduced,in which the it pre-computes sum and carry for the two possible cases i.e., for carry =0 and carry=1.For a 16 bit carry select adder in fig.2 the first 8 LSB,s are designed as in ripple carry adder with carry in as '0' ,and the 8 MSB's are designed by assuming once carry as '0' and later carry as '1' .Depending upon the carry from the last LSB,whether carry is '0' or '1' the particular set of MSB is selected and the sum and carry is generated using the multiplexers.This pre-computation reduces the delay of rippling of carry which is limited to only one multiplexer of each stage.Hardware requirement for Carry Select Adder is more when compared to that of ripple carry adder even though it gives less delay.Thus, there is a tradeoff between area and delay.

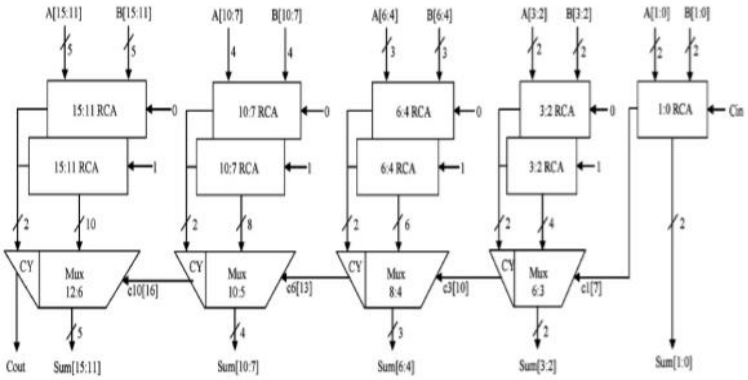


Fig.2 : 16-bit Carry Select Adder

3. CONVENTIONAL CSLA DESIGN

As we know , for a CSLA to be designed ,consists of 2 basic blocks.They are Full Adder and Multiplexer.

3.1 Full Adder:

The full adder that is used in this is the conventional CMOS full adder as shown in fig.3 .

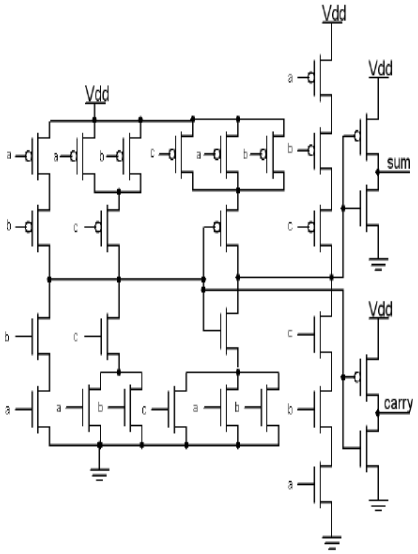


Fig.3 : Schematic of Full Adder

The Sum and Carry can be implemented is full adder is as shown below.
Sum=A ⊕ B ⊕ C_{in}
Carry= (A . B)+ (C_{in} . (A ⊕ B))

3.2 Multiplexer
In electronics MUX is a device which selects one of many input signals and forwards the selected input to the output.The selection of input is done by selection line.For a 2^n input MUX has n selection lines.In this CSLA design 2X1 MUX is used as shown in fig.4.Depending on the selection line 'S' any one of the inputs is selected.

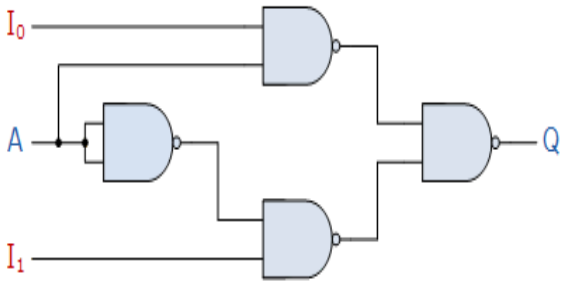


Fig.4: Gate Level 2X1 Multiplexer

3.3 Implementation
In this,the total CSLA design is divided into two parts.The design is a uniform CSLA design in which total number of bits are divided into equal number of LSB's(8) and MSB's(8) .The MSB is designed in such a way that carry in is presumed as '0' and '1'.This CSLA is designed by taking the conventional full adder as previously shown.The tpology of the Carry select adder using conventional full adder is shown in fig.5.

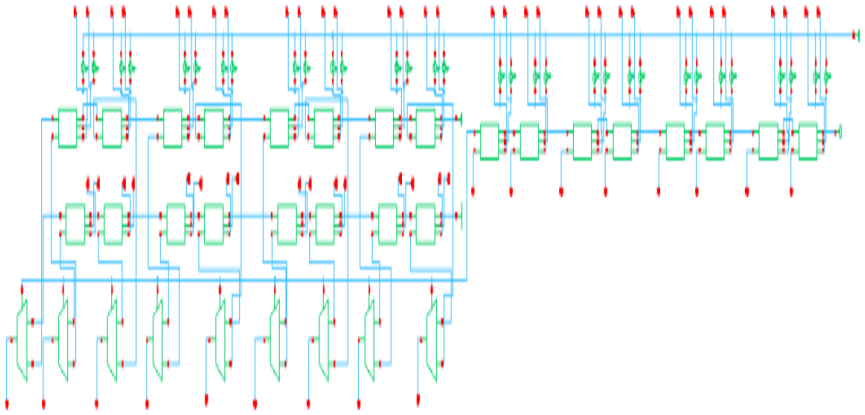


Fig.5: Conventional CSLA Topology

4. PROPOSED CSLA DESIGN
In this proposed CSLA design,instead of using conventional full adder ,a new type of full adder which is fully symmetric bridge structure is used.These bridge circuits has symmetrical pull-up and pull down sections.With these symmetrical structures low power can be achieved at lower technology nodes.These symmetrical structures are so robust and can be implemented with less number of transistors than the conventional counterparts.

4.1 Bridge Style Circuits
Bridge circuits are circuits that create a conditional conjunction between two circuit nodes. Using this kind of circuits the classical circuits can be implemented faster and smaller than the conventional. Since one of the important parameters in circuit design is the chip area, the proposed style might reduce area or increase density of transistors in unit of area.
If a function has 2^{n-1} logical '0's and 2^{n-1} logical '1's can be implemented in fully symmetrical style,that means not every logical function can be implemented in this style[1].As mentioned before regular CMOS design style performs realizations by organizing some different branches which provides a path from supply to the ground,whereas bridge style focuses its attention to meshes and connectes each mesh by a transistor known as 'bridge transistor'. This bridge transistors provide the

possibility of sharing transistors of different paths to create a new path from supply line to ground.These transistors not only validate the correctness of the circuit but also preserves the pull-up and pull-down mutually exclusive.

As previously discussed only certain logic functions can be implemented in bridge style.As the full adder totally meets the design criteria i.e., which has 2^{n-1} logical '0's and 2^{n-1} logical '1's in its sum and carry function,it can be implemented as a fully symmetrical bridge style circuit.The sum and the carry functions can be separately implemented. Fig.6 illustrates the design of sum function in bridge form.

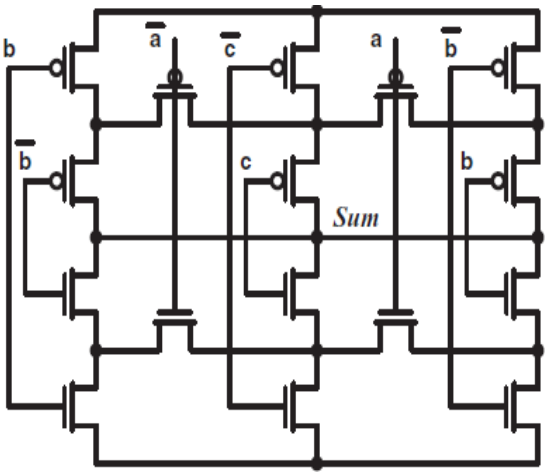


Fig.6 : Bridge implementation of SUM Function

The Sum function can be given as

$$\overline{\text{Sum}}(a,b,c) = m_0 + m_3 + m_5 + m_6 = \bar{a}.\bar{b}.\bar{c} + \bar{a}.b.c + a.\bar{b}.c + a.b.\bar{c}$$

The carry function also meet the bridge style design criteria and can be implemented as shown in fig.7.The Carry function is given by

$$\overline{\text{Carry}}(a,b,c) = m_0 + m_1 + m_2 + m_4 = \bar{a}.\bar{b}.\bar{c} + \bar{a}.\bar{b}.c + \bar{a}.b.\bar{c} + a.\bar{b}.\bar{c}$$

The bridge style circuits can be categorized into two structures. One of them is fully-symmetric style and another one is semi-symmetric. This categorization is based on the similarities amount of P and N networks implementation. If the implementation of P and N is fully-similar then the style of circuit is fully-symmetric, and if those implementations are not similar then we could say it is semi-symmetric.

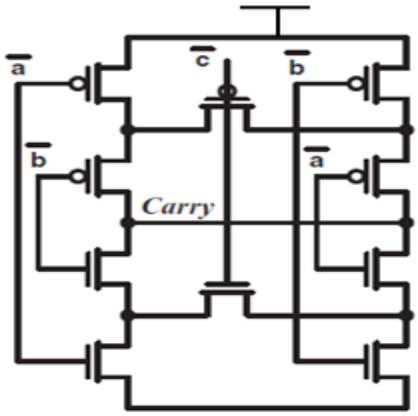


Fig.7: Bridge implementation of CARRY Function

In order to design Carry Select Adder a multiplexer is used to select the desired sum.To achieve low power and efficiency a tranmisssion gate MUX is used as shown in fig.8.

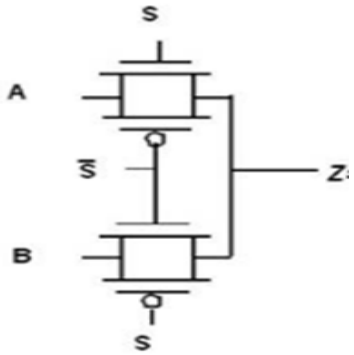


Fig.8 : TG 2X1 Multiplexer

The transmission gate multiplexer selects any one of the input depending on the select line. The transmission gate selects input A or B on the basis of the value of the control signal S. When S=0, Z=A and when S=1, Z=B.
Z = A.S + B.S

4.2 Implementation of Proposed CSLA
The proposed CSLA topology is similar to that of the conventional one as shown in fig.9.They differ in the type of full adder and the multiplexer used in order to achieve low power.

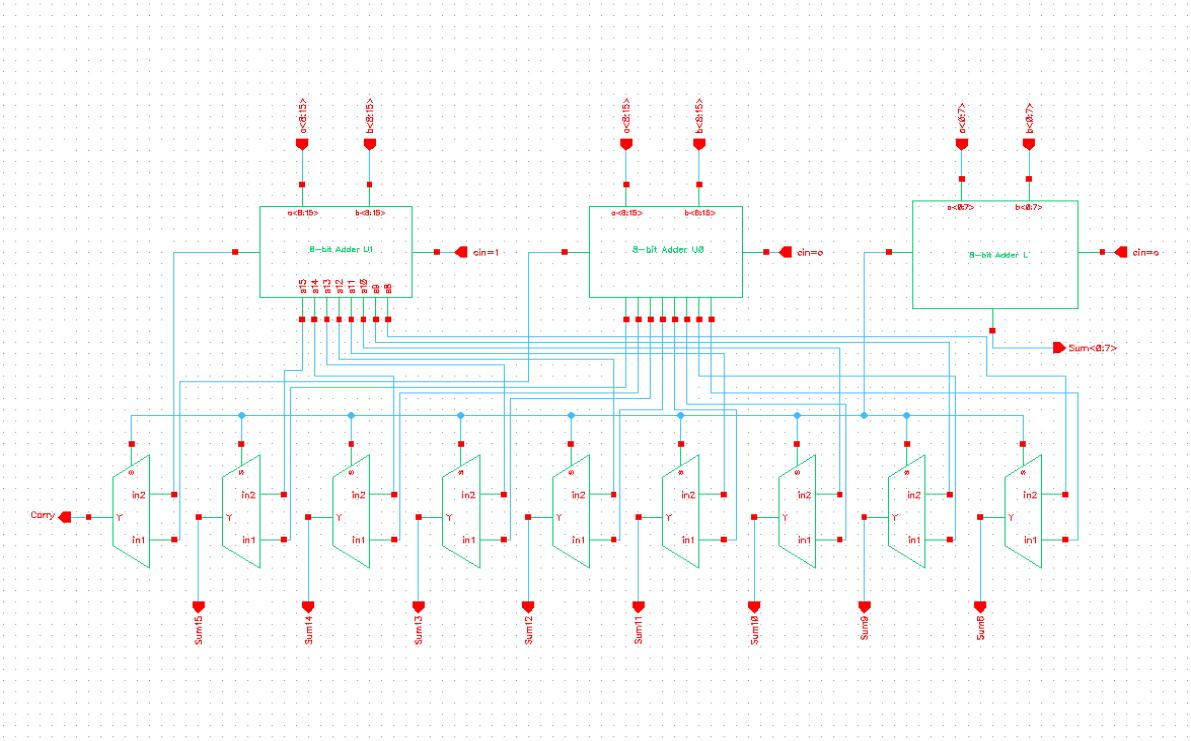
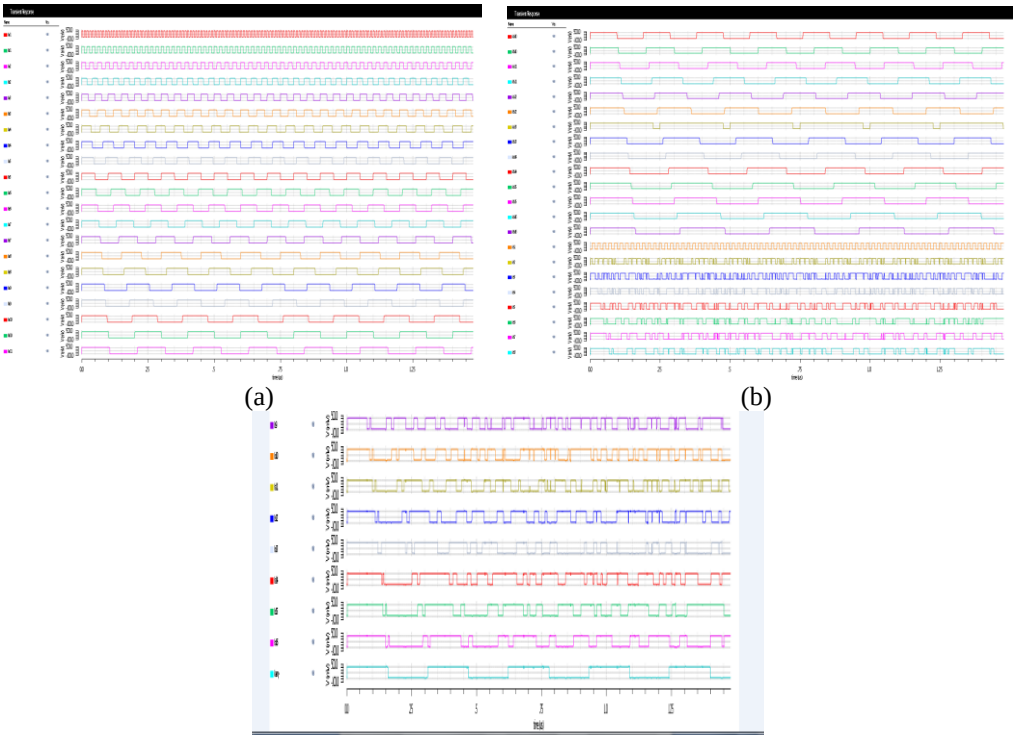


Fig.9 : Proposed CSLA Topology

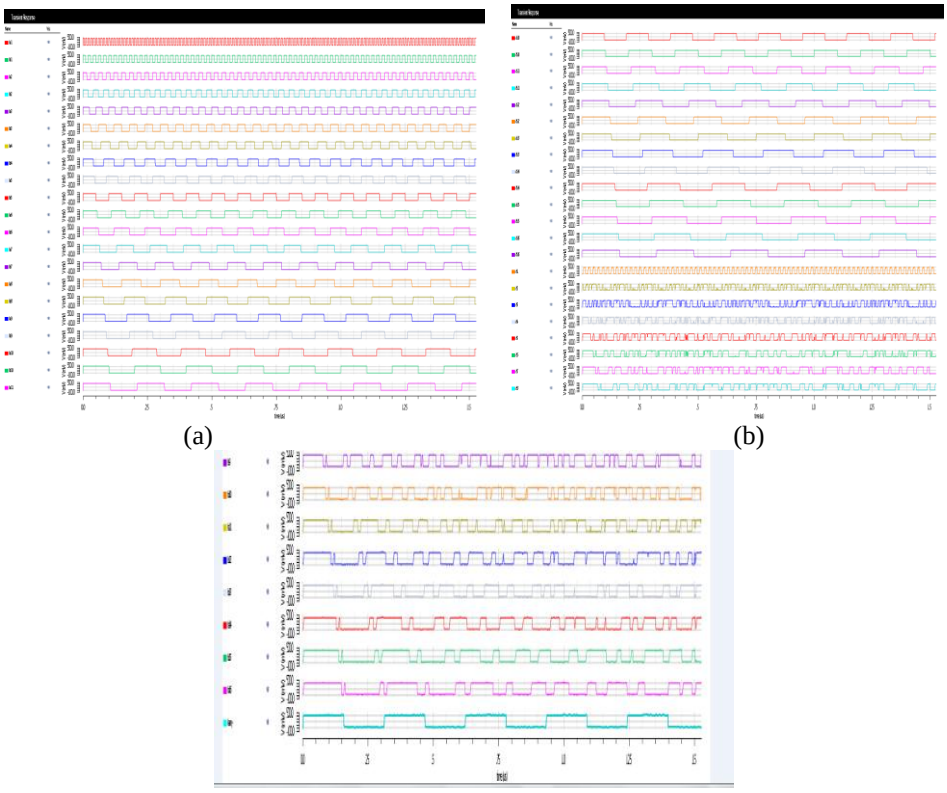
5. SIMULATION RESULTS AND DISCUSSION
All the circuits are designed in Cadence Virtuoso environment using CMOS gpdk 90nm .Both the circuits are simulated with specific voltage and temperature.The power consumption that is calculated as the average which ensures the accurate power consumption of the circuit.The propogation delays are separately measured for both the sum and carry signals.Finally the Power Delay Product(PDP) is calculated as the product of worst case delay and the average power consumption.In addition to power and delay layouts of both the conventional and proposed design are shown.The simulation results are listed in Table 1.
The Input and Output signal patterns are shown for conventional in fig 10.(a),(b),(c) and for proposed design are shown in fig 11.(a),(b),(c) respectively.



(a) (b)

(c)

Fig.10: Simulated signal patterns of Conventional CSLA



(a) (b)

(c)

Fig.11: Simulated signal patterns of Proposed CSLA

5.1 Layouts

The layouts for the conventional CMOS full adder and bridge style full adder are drawn and evaluated.The bridge style cell occupies less area when compared to normal one as it contains less number of transistors.And the extraction also shows less number of parasitics in bridge style full adder.The layout for regular CMOS and bridge style full adder are shown in fig.12 and fig.13 respectively.

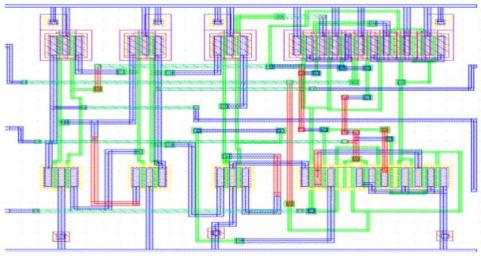


Fig.12: Layout of Conventional CMOS Full Adder

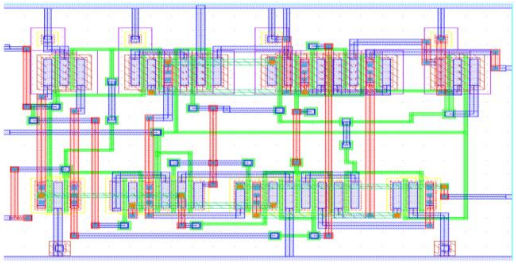


Fig.13: Layout of bridge style Full Adder

6. CONCLUSION AND FUTURE WORKS

This paper investigates the design of novel 16 bit CSLA using a highly robust fully symmetrical bridge circuit.In order to still achieve low power a TG gate Multiplexer is used than a conventional CMOS one.This combination reduces the power consumption greatly and achieves high performance.The simulated results show that the power for the proposed CSLA has reduced by 28.56% comparing to the conventional CSLA.The delay has also significantly reduced.In addition to this both the area and PDP also significantly affected by using this fully bridge style adder cell. These bridge style circuits can be easily fabricated as the lower or NMOS section is the exact replica of the PMOS section. Hence,by employing bridge style circuits energy savings in larger designs will be greatly improved at lower technology nodes.

Table 1.Comparison of Simulation Results

Design	Width	Power (n W)	Delay (n s)	PDP (f J)
Conventional CSLA	4 bit	414.3	78.41	32.485
	8 bit	635.7	228.0	144.939
	16 bit	861.4	469.5	404.427
Proposed CSLA	4 bit	316.6	77.11	24.413
	8 bit	467.8	77.76	36.376
	16 bit	614.6	158.8	97.598

7. REFERENCES

[1] Reza Faghih Mirzaee, Masoomeh Jasemi, Ali Valizadeh and Nader Bagherzadeh “On the design of fully symmetrical bridge-style circuits” IETE JOURNAL OF RESEARCH, 2015.

[2] M. Vinod Kumar Naik, Mohammed Aneesh. Y,” Design of Carry Select Adder for Low-Power and High Speed VLSI Applications”, 2015 IEEE International Conference on Electrical,C omputer and Communication Technologies (ICECCT),pp 1-4.

[3] Keivan Navi, Omid Kavehie, Mahnoush Rouholamini, Amir Sahafi and Shima Mehrabi,” A Novel CMOS Full Adder”,IEEE, 20th International Conference on VLSI Design.

[4] K. Swarna Madhuri, M. Madhu Sudhan Reddy,” Low-Power and High-Performance 1-Bit CMOS Full-Adder Cell”, International Journal of Science and Research (IJSR).

[5] Phaniram Sayapaneni, V Elamaran,” A Comparative Study on Low Power Adders using Microwind EDA Tool”,IEEE 2014, International Conference on Computational Intelligence and Computing Research.

[6] B. Sathyabhama, M. Deepika, and S. Deepthi,” Area and Power Efficient Carry Select Adder using 8T Full Adder”, IEEE ICCSP 2015.

[7] Amit Grover and Neeti Grover ,” Comparative Analysis: Area-Efficient Carry Select Adders 180 nm Technology”, 2013 7th Asia Modelling Symposium.

[8] Shivendra Pandey, Afshan Amin Khan and Rajkumar Sarma,” Comparative Analysis of Carry Select Adder using 8T and 10T Full Adder Cells”, IEEE, International Conference on Communication and Signal Processing, April 3-5, 2014.

[9] A. Ramakrishna Reddy M.Parvathi,” Efficient Carry Select Adder using 0.12µm Technology for Low Power Applications”,IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI),2013.

[10] Ms. Anagha U P, Mr. Pramod P,” Power and Area Efficient Carry Select Adder”, IEEE Recent Advances in Intelligent Computational Systems (RAICS), December 2015.

[11] Mariano Aguirre-Hernandez and Monico Linares-Aranda,” CMOS Full-Adders for Energy-Efficient Arithmetic Applications”, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 19, NO. 4, APRIL 2011.

[12] Rohan Jain, Prateek Singh, Anmol Sharma, Rajiv Sharma,” Design, Simulation and Analysis of Energy Efficient 1-Bit Full Adder at 90nm CMOS Technology for Deep Submicron Levels”,IEEE, International Conference on Computing, Communication and Automation (ICCCA2016).

[13] Anjali Sharma, Richa Singh, Rajesh Mehra,” Low Power TG Full Adder Design Using CMOS Nano Technology,” 2012 2nd IEEE International Conference on Parallel, Distributed and Grid Computing.

[14] T.Abhiram, T. Ashwin,,” Modified carry select adder for power and area reduction,”IEEE, 2017 International Conference on Circuit ,Power and Computing Technologies (ICCPCT).